LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A DC-DC converter comprising:

a synchronous semiconductor device; and

a control semiconductor device;

wherein at least one of said semiconductor devices includes:

a semiconductor body of a first conductivity which includes a channel region of a second conductivity and a major surface;

an active region formed in said semiconductor body, said active region including a trench less than 0.5 microns wide extending through said channel region and a gate structure disposed in said trench which includes a gate oxide layer disposed at least on said sidewalls of said trench and a gate electrode disposed adjacent said gate oxide layer; and

a termination structure, said termination structure including,

a termination trench formed in said semiconductor body, and a field oxide layer formed in said termination trench below said major surface, wherein said field oxide layer is thicker than said gate oxide layer.

2. Canceled.

3. Canceled.

4. (Previously Presented) A semiconductor device according to claim 1, wherein said trench include an oxide mass formed at its bottom said oxide mass being thicker than said gate oxide layer.

5. (Original) A semiconductor device according to claim 4, wherein said semiconductor body includes conductive regions of said first conductivity formed adjacent said trench in said channel region, and further comprising a semiconductor substrate of said conductivity, said semiconductor body being formed over said semiconductor substrate, wherein

said conductive regions are electrically connectable to said semiconductor substrate through invertible channels adjacent said trench.

6. (Original) A semiconductor device according to claim 5, wherein said conductive regions are source regions.

7. (Previously Presented) A semiconductor device according to claim 1, wherein the depth of said trench has been selected to achieve an optimum figure of merit.

8. (Previously Presented) A semiconductor device according to claim 1, wherein said trench is a stripe.

9. (Previously Presented) A semiconductor device according to claim 1, wherein said trench is a cell.

10. (Original) A semiconductor device according to claim 9, wherein said cell is hexagonal.